

ESKISEHIR TECHNICAL UNIVERSITY
DEPARTMENT OF ELECTRICAL AND ELECTRONICS
ENGINEERING

LAB-1
A 4-BIT SEQUENTIAL ADDER

1 Introduction

As an introduction to VHDL, you will implement a sequential adder based on the structure given in this document.

2 Addition of Signed Numbers

Addition of signed numbers is not significantly different from addition of unsigned numbers. Recall that signed 4 bit numbers (2's complement) can represent numbers between -8 and 7. Let's remember how this addition works, consider three examples given below.

Decimal	Signed Binary
	<i>1110</i> (carry)
-2	1110
<u>+3</u>	<u>+0011</u>
1	0001

Decimal	Signed Binary
	<i>011</i> (carry)
-5	1011
<u>+3</u>	<u>+0011</u>
-2	1110

Decimal	Signed Binary
	<i>1100</i> (carry)
-4	1100
<u>-3</u>	<u>+1101</u>
-7	1001

There are two ways to get an overflow while adding two signed numbers. -- if the result is greater than 7, or less than -8. If two numbers with the same sign (either positive or negative) are added and the result has the opposite sign, an overflow has occurred.

3 Sequential Adder

A sequential adder requires additional signals for synchronization purpose.

Input **CLK**: clock signal to synchronize the system.

Input **RESET**: asynchronous reset signal to initialize the system.

Input **STARTA**: synchronous signal that must be high to start taking input **A**.

Input **LOADB**: synchronous signal that must be high to load the value of **B**.

Output **STARTC**: synchronous signal that is set during 1 cycle by the adder when the result of the operation is available on output **C**.

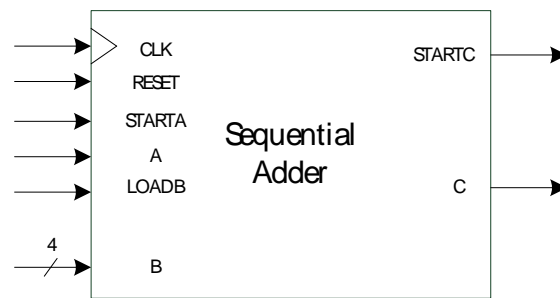


Figure 1: Block diagram of the sequential adder.

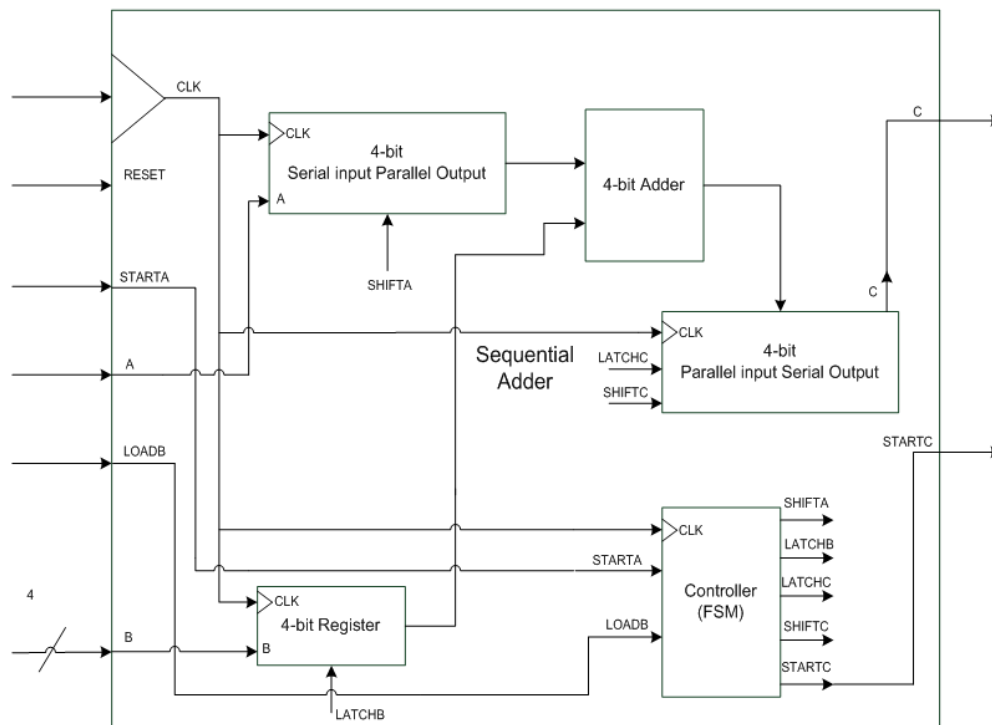


Figure 2: Internal structure of the 4-bit sequential adder.

To implement the sequential adder, we will use the algorithm described here. In this algorithm, Input B is loaded in parallel to the register in the system. Input A is taken in serial to the register in the system. When receiving the value of A is completed, addition operation gives correct result at the output of the adder. The result is then transmitted to the output C serially. STARTC output signal is set to high to indicate that the result of the operation is available at the output C.

The 4-bit SIPO (Serial Input Parallel Output) gets the most significant bit first; hence it shifts left, not right. The controller generates all internal and external control signals. You should remember a combinational parallel adder and you should use that component in here.

Value A arrives in series, bit after bit, with the MSB first. The arrival of a new value A is pointed out by the activation of a signal *STARTA* during the first bit of A (MSB).

Value B arrives always before the first bit of value A. It arrives to the system in parallel, the four bits at once. Its arrival is pointed out by the activation of signal *LOADB*.

The four bits of the result C are sent to the output in series, bit after bit, with the least significant bit first. The output of a new result on C is pointed out by the activation of a signal *STARTC* during the first bit of C (the LSB). Value C is sent to the output in series with least significant bit first.

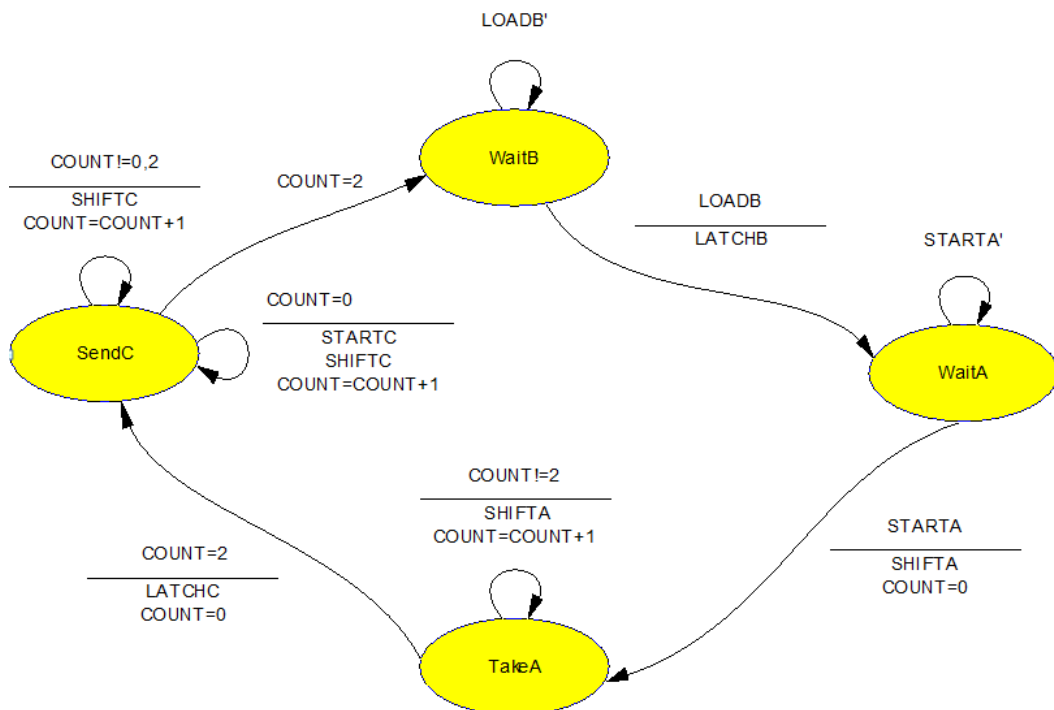
A new value B is ignored while the previous computation is taking place (from the time *STARTA* is activated to the moment the last bit of C is output).

RESET signal is used initialize the adder. When *RESET* signal is set to zero, the registers inside the system is initialized to 0 and state of the system is set to start state.

The system Controller contains a state machine, and it sets the control signals of all the components inside system.

4 Finite State Machine

The controller contains the following state machine. It includes a counter used to count the 3 steps of the addition algorithm.



Note that: $STARTA'$ = The Inverse of the $STARTA$ signal , $LOADB'$ = The Inverse of the $LOADB$ signal.

5 Procedure

You have to recall your knowledge about using ISE from EEM334 Digital Systems II Labs. In this first lab, you will design a synchronous system to compute $C=A+B$, where the 3 values are signed integers on 4 bits.

- Write the VHDL description of the system described above.
- You should simulate your design using ISE or another VHDL simulator.