Instruction Cyles (Single Oper.)

Number of cycles for Format II					
Addr. Mode	RRA,RRC,SWPB,SXT	PUSH	CALL	Size	Operation
Rn	1	3	4	1	**SWP R5**
@Rn	3	4	4	1	**RRC @R9**
@Rn+	3	5	5	1	**SWPB @R10+**
#N	Don't use	4	5	2	**CALL #04000h**
x(Rn)	4	5	5	2	**CALL 2(R7)**
EDE	4	5	5	2	**PUSH EDE**
&EDE	4	5	5	2	**SXT &EDE**

Instruction Cycles (Double Oper.)

Number of Cycles for Instruction Format I				
Addressing Mode				
Source	Destination	No of Cycles	Size	Operation
Rn	**Rm**	1	1	**MOV R6,R11**
	PC	2	1	**BR R10**
	X(Rm)	4	2	**ADD R5,8(R9)**
	EDE	4	2	**XOR R7,EDE**
	&EDE	4	2	**MOV R6,&EDE**
@Rn	**Rm**	2	1	**AND @R3,R7**
	PC	2	1	**BR @R11**
	X(Rm)	5	2	**XOR @R5, 4(R7)**
	EDE	5	2	**MOV @R8,EDE**
	&EDE	5	2	**XOR @R7,&EDE**

Instruction Cycles (Double Oper.)

Number of Cycles for Instruction Format I				
Addressing Mode				
Source	Destination	No of Cycles	Size	Operation
@Rn+	**Rm**	2	1	**ADD @R6+,R11**
	PC	3	1	**BR @R10+**
	X(Rm)	5	2	**ADD @R7+,8(R9)**
	EDE	5	2	**XOR @R7+,EDE**
	&EDE	5	2	**MOV @R6+,&EDE**
#N	**Rm**	2	1	**MOV @22,R7**
	PC	2	1	**BR #05252h**
	X(Rm)	5	2	**MOV #48,0(SP)**
	EDE	5	2	**ADD #44,EDE**
	&EDE	5	2	**ADD #48,&EDE**

Instruction Cycles (Double Oper.)

Number of Cycles for Instruction Format I				
Source	Destination	No of Cycles	Size	Operation
X(Rn)	**Rm**	3	2	**ADD 2(R6),R11**
	PC	3	2	**BR 2(R10)**
	X(Rm)	6	3	**ADD 4(R7),8(R9)**
	EDE	6	3	**MOV 4(R11),EDE**
	&EDE	6	3	**MOV 4(R6),&EDE**
SRC	**Rm**	3	2	**ADD SRC,R7**
	PC	3	2	**BR SRC**
	X(Rm)	6	3	**MOV SRC,0(SP)**
	DEST	6	3	**CMP SRC,DEST**
	&DEST	6	3	**ADD SRC,&DEST**

Instruction Cycles (Double Oper.)

Number of Cycles for Instruction Format I				
Source	Destination	No of Cycles	Size	Operation
&SRC	**Rm**	3	2	**ADD &SRC,R11**
	PC	3	2	**BRA &SRC**
	X(Rm)	6	3	**MOV &SRC,0(R11)**
	DEST	6	3	**MOV &SRC,DEST**
	&DEST	6	3	**MOV &SRC,&DEST**

Instruction Cycles (examples)

Instruction	Fetch cycles	Operand fetch cycle	Result store cycle	Additional cycles*	Total cycles
`add r5,r6`	1	0	0	0	1
`add &SRC,r6`	2	1	0	0	3
`add #100,r6`	2	0	0	0	2
`add r5,DEST`	2	1	1	0	4
`add SRC,DEST`	3	2	1	0	6
`cmp SRC,r6`	2	1	0	0	3
`jmp label`	1	0	0	1	2
`mov r5,pc`	1	0	0	1	2
`pop pc`	1	1	0	1	3
`pop r5`	1	1	0	0	2
`push r5`	1	0	1	1	3
`push #0x1234`	2	0	1	1	4
`Call #0x1234`	2	0	1	2	5

* Additional cycles to perform internal processing