ESKİŞEHİR TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EEM 334 Digital Systems II

LAB 7 – FSM SEQUENCE DETECTOR

1. PURPOSE

In this lab, you will design and implement FSM circuit of a sequence detector. The circuit that you will design will have the following characteristics. The block diagram of the circuit is given in Figure 1.

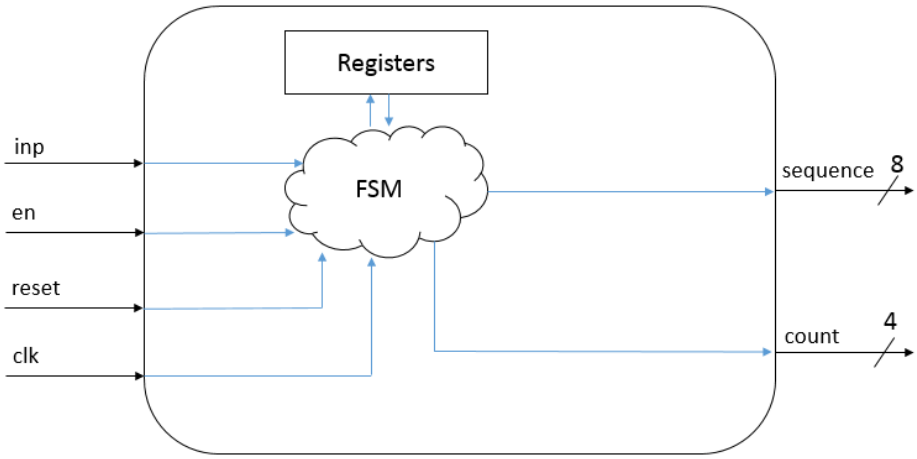

Figure 1. Block diagram of sequence detector top.vhd

The design will have 1-bit serial data input (inp), 1-bit active-high enable (en), and asynchronous reset inputs in addition to the clock input. Your outputs will be a 8-bit sequence which represents the latest 8 inputs and a 4-bit count that shows the number of detected sequences

2. BACKGROUND

A finite-state machine (FSM) or simply a state machine is used to design both computer programs and sequential logic circuits. It is conceived as an abstract machine that can be in one of a finite number of user defined states. The machine is in only one state at a time; the state it is in at any given time is called the current state. It can change from one state to another when initiated by a triggering event or condition; this is called a transition. A particular FSM is defined by a list of its states, and the triggering condition for each transition. While designing FSM, you should follow some steps;

Step 1: Describe the machine in words.
Step 2: Draw the FSM diagram
Step 3: Write state table (if it is required)
Step 4: Write VHDL code
Step 5: Simulate and implement the circuit

The state machines are modeled using two basic types of sequential networks- Mealy and Moore. In a Mealy machine, the output depends on both the present (current) state and the present (current) inputs. In Moore machine, the output depends only on the present state.

Mealy Machine

A general model of a Mealy sequential machine consists of a combinatorial network, which generates the outputs and the next state, and a state register which holds the present state as shown below. The state register is normally modeled as D flip-flops. The state register must be sensitive to a clock edge.

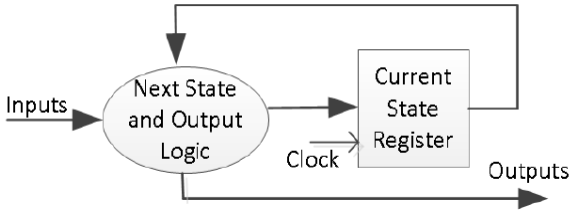

Figure 2. Two-block Mealy machine

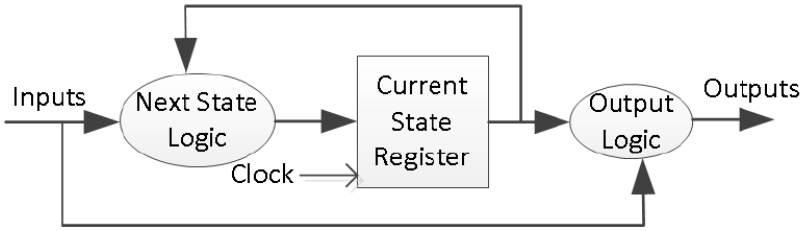

Figure 3. Three-block Mealy machine

Moore Machine

A general model of a Moore sequential machine is shown Figure 4. Its output is generated from the state register block. The next state is determined using the present (current) input and the present (current state). Here the state register is also modeled using D flip-flops.

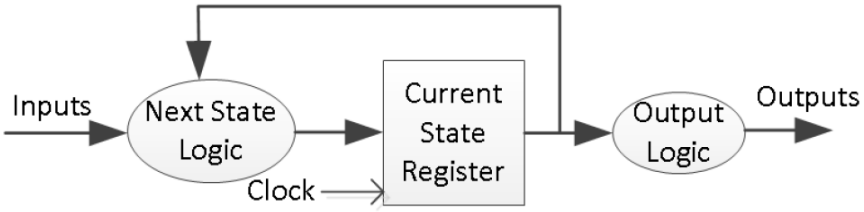

Figure 4. Three-block Moore machine

3. PROCEDURE

You will design a Moore type sequence detector circuit according to the following specifications: It samples 1-bit serial data input coming from the user assigned testbench codes.

Your FSM circuit will search the pattern **1101** on the serial data input if the active-high enable signal is asserted. The end of one pattern can be the start of another. For example, your circuit should detect the search pattern twice for the input sequence of 1101101.

An asynchronous reset will put your circuit into a reset state, and clear all registers and outputs.

Steps:

1. Design your FSM
2. Create top module and instantiate the components if necessary
3. Code your FSM, make necessary connections between components and ports.
4. Create a simulation to verify the functionality of the design.
5. Create .ucf file and assign the ports to pins.
6. Load the design on FPGA.
7. Verify your results and show them to your assistant.

You can take advantage of the Xilinx example designs. You can access them by using language templates in edit menu of the ISE editor.