EXPERIMENT 3:
Quadrature Phase Shift Keying (QPSK)

1) OBJECTIVE

Generation and demodulation of a quadrature phase shift keyed (QPSK) signal.

2) PRELIMINARY DISCUSSION

QPSK is a form of phase modulation technique, in which two information bits (combined as one symbol) are modulated at once, selecting one of the four possible carrier phase shift states. Recall that in binary PSK (BPSK), the change in logic level causes the BPSK signal's phase to change, it does so by 180^o. Figure 1 illustrates a BPSK signal (lower), together with the modulating binary sequence (upper).

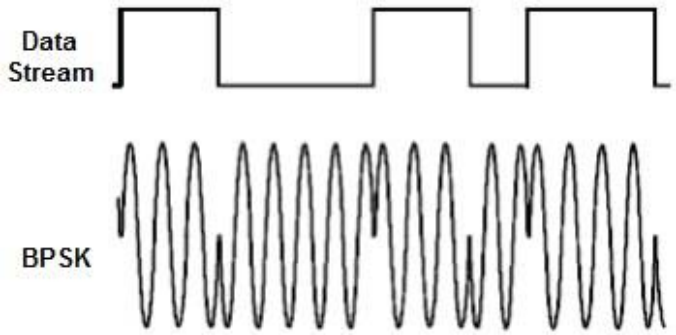

Figure 1: a BPSK signal (below) and the message (above)

A QPSK signal can be generated by independently modulating two carriers in quadrature as shown in Figure 2.

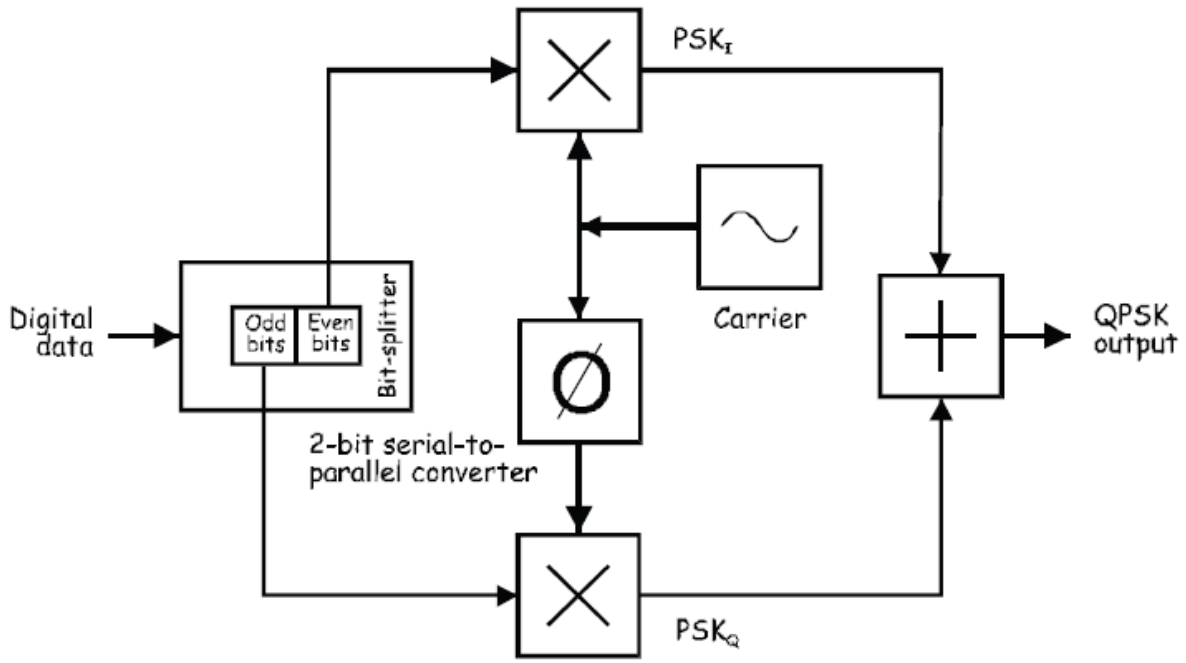

Figure 2: Block diagram of the mathematical implementation of QPSK

At the input to the modulator, the digital data's even bits (that is, bits 0, 2, 4 and so on) are stripped from the data stream by a "bit-splitter" and are multiplied with a carrier to generate a BPSK signal (called PSK_I). At the same time, the data's odd bits (that is, bits 1, 3, 5 and so on) are stripped from the data stream and are multiplied with the 90° phase-shifted carrier to generate a second BPSK signal (called PSK_Q). The two BPSK signals are then simply added together for transmission. Figure 3 illustrates this procedure to generate a QPSK signal.

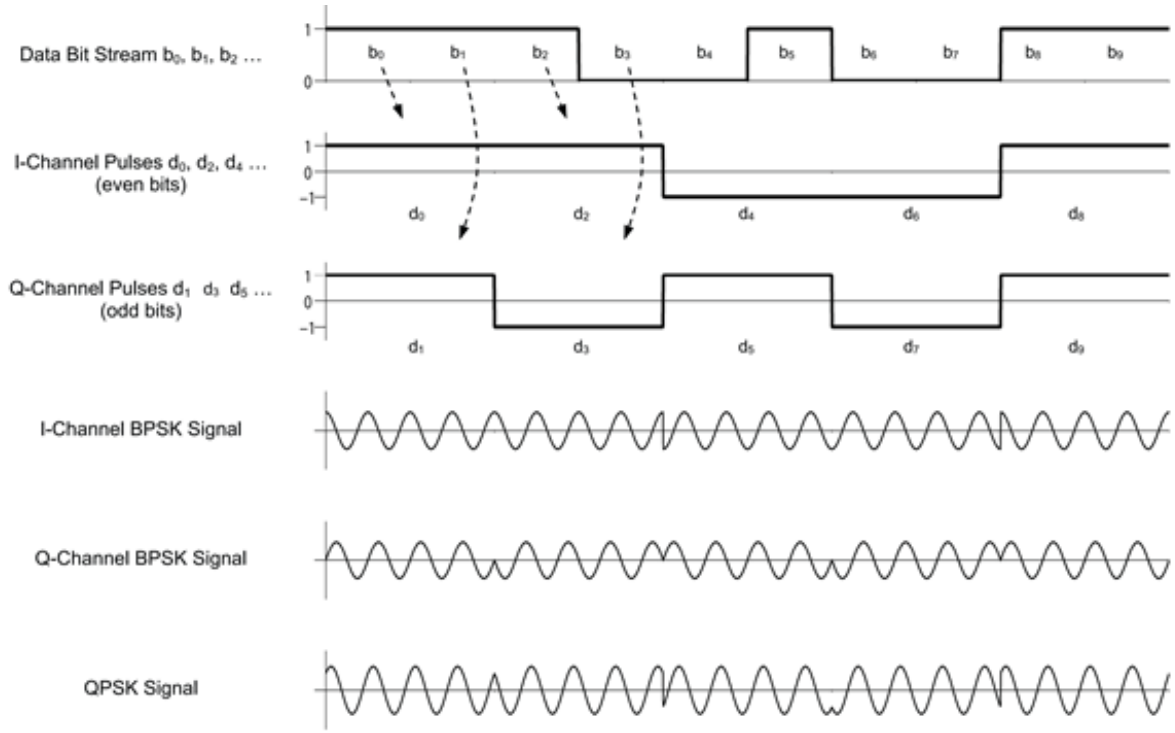

Figure 3: QPSK signal generation from two BPSK signals

The 90º phase separation between the carriers allows the sidebands to be separated by the receiver using phase discrimination. Figure 4 shows the block diagram of the mathematical implementation of QPSK demodulation.

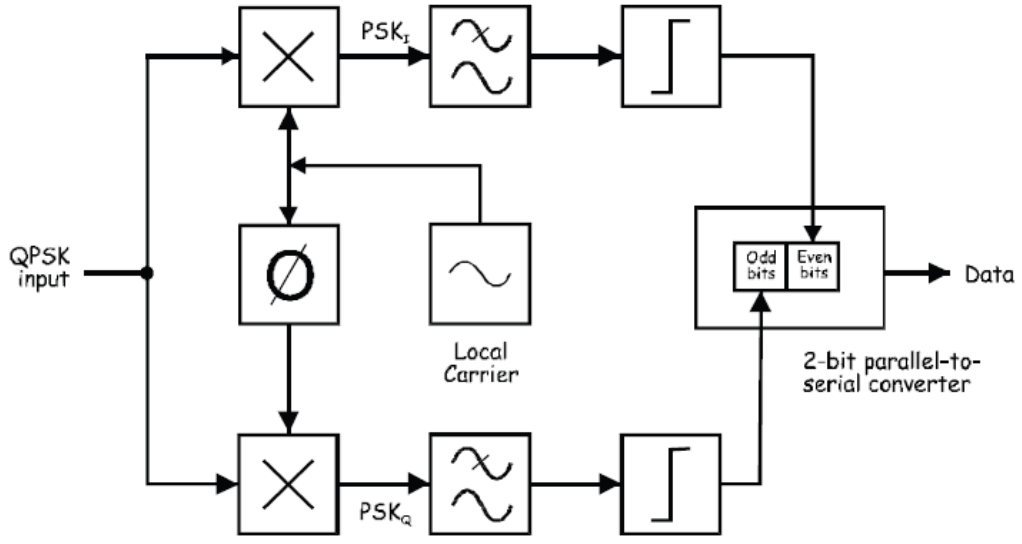

Figure 4: Block diagram of the mathematical implementation of QPSK demodulation

Notice the arrangement uses two product detectors to simultaneously demodulate the two BPSK signals. This simultaneously recovers the pairs of bits in the original data. The two signals are cleaned-up using a comparator or some other signal conditioner then the bits are put back in order using a 2-bit parallel-to-serial converter.

3) LAB WORK

In this experiment you'll use the Emona Telecoms-Trainer 101 to generate a QPSK signal by implementing the mathematical model of QPSK. Once generated, you'll examine the QPSK signal using the scope. Then, you'll examine how phase discrimination using a product detector can be used to pick-out the data on one BPSK signal or the other.

Equipment

- Emona Telecoms-Trainer 101 (plus power-pack)
- Dual channel 20MHz oscilloscope
- Three Emona Telecoms-Trainer 101 oscilloscope leads
- Assorted Emona Telecoms-Trainer 101 patch leads

Procedure

Part A – Generating a QPSK signal

1. Set the scope's CH1 and CH2 Input Coupling controls to the DC position.
2. Set the scope's Timebase control to the 0.5 ms/div position.
3. Locate the Divider module and set it up to divide by 2 pushing the left-side switch up and the right-side switch down.
   Tip: The Divider module is underneath the Sequence Generator module.
4. Connect the set-up shown in Figure 5.
   Note: Insert the black plugs of the oscilloscope leads into a ground (GND) socket.

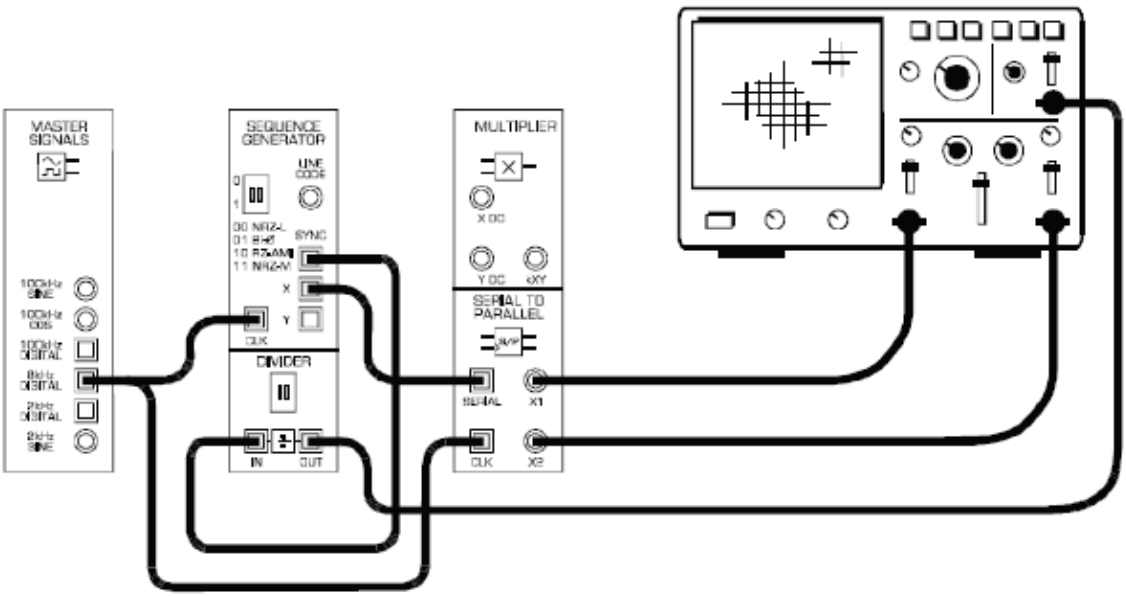

Figure 5: the set-up for a serial-to-parallel conversion

The block diagram in Figure 6 below can represent the set-up in Figure 5. The Sequence Generator module is used to model digital data. The 2-bit Serial-to-Parallel Converter module is used to split the data bits up into a stream of even bit and odd bits.

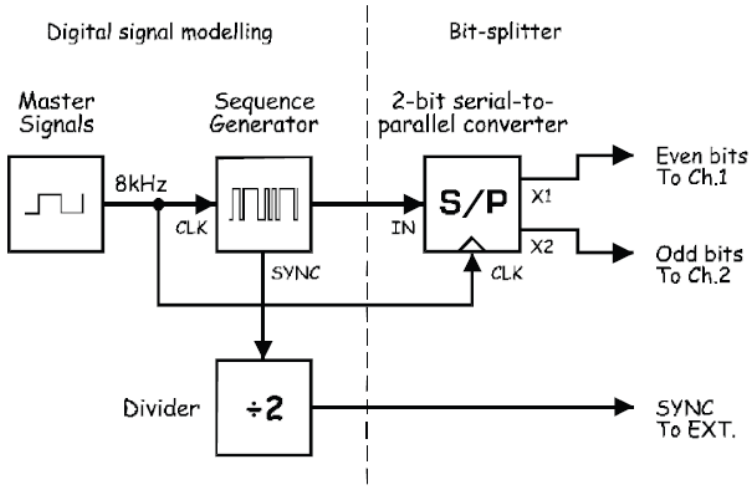

Figure 6: block diagram of Figure 5

5. Set the scope's Mode control to the DUAL position to view the Serial-to-Parallel Converter module's two outputs.
6. Compare the signals. You should see two digital signals that are different to each other.

Question 1

What is the relationship between the bit rate of these two digital signals and the bit rate of the Sequence Generator module's output?

1. Modify the set-up as shown in Figure 7 below.
   Remember: Dotted lines show leads already in place.

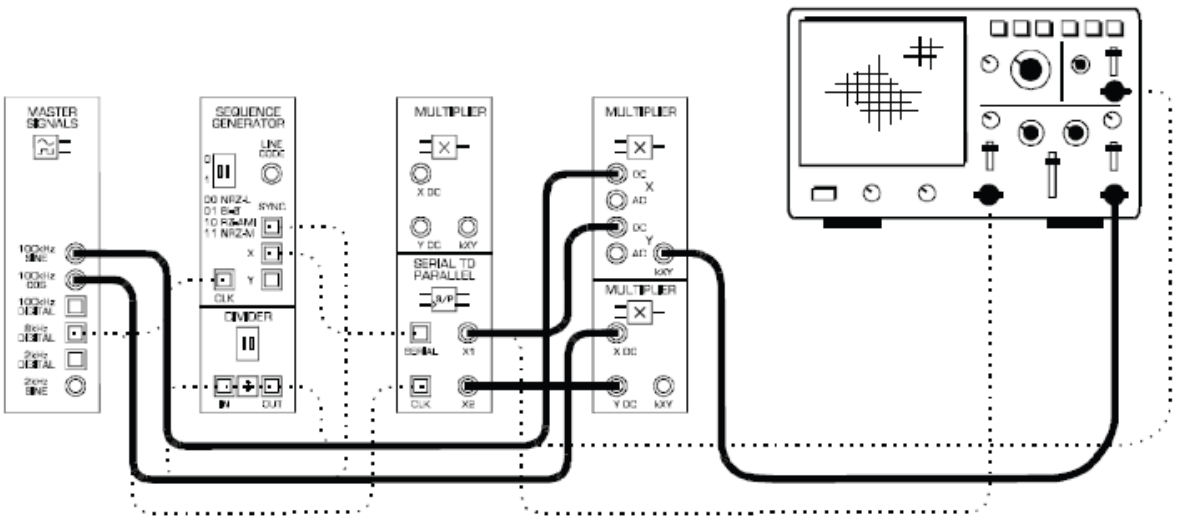

Figure 7: the set-up for the generation of PSK_I

Excluding the digital data modelling, the set-up in Figure 7 can be represented by the block diagram in Figure 8 below.

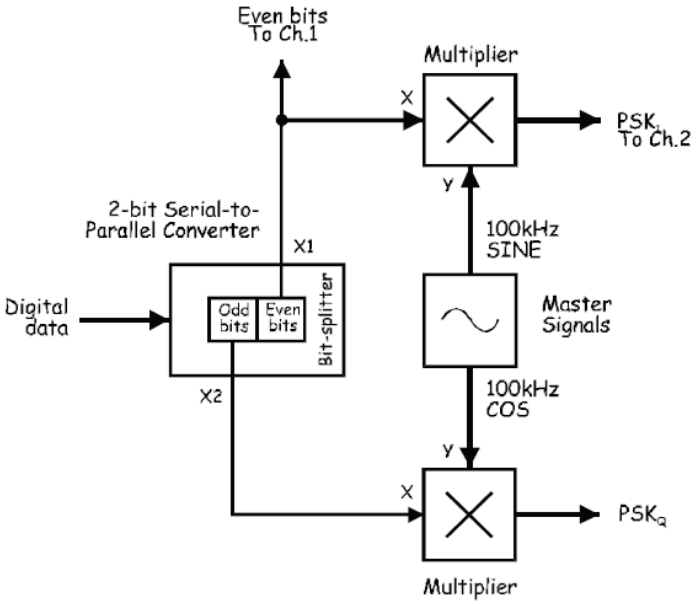

Figure 8: block diagram of Figure 7

2. Compare the even bits of data with the Multiplier module's output (PSK_I).
3. Set the scope's Timebase control to the 200 µs/div position.
4. Activate the scope's Sweep Multiplier to view the signals more closely.
5. Use the scope's Horizontal Position control to locate a transition in the data sequence.
6. Examine the carrier and look closely at the way it changes at the sequence's transitions.

Question 2

What feature of the Multiplier's output suggests that it's a BPSK signal?

7. Deactivate the scope's Sweep Multiplier.
8. Move the scope's connections as shown in Figure 9 below.

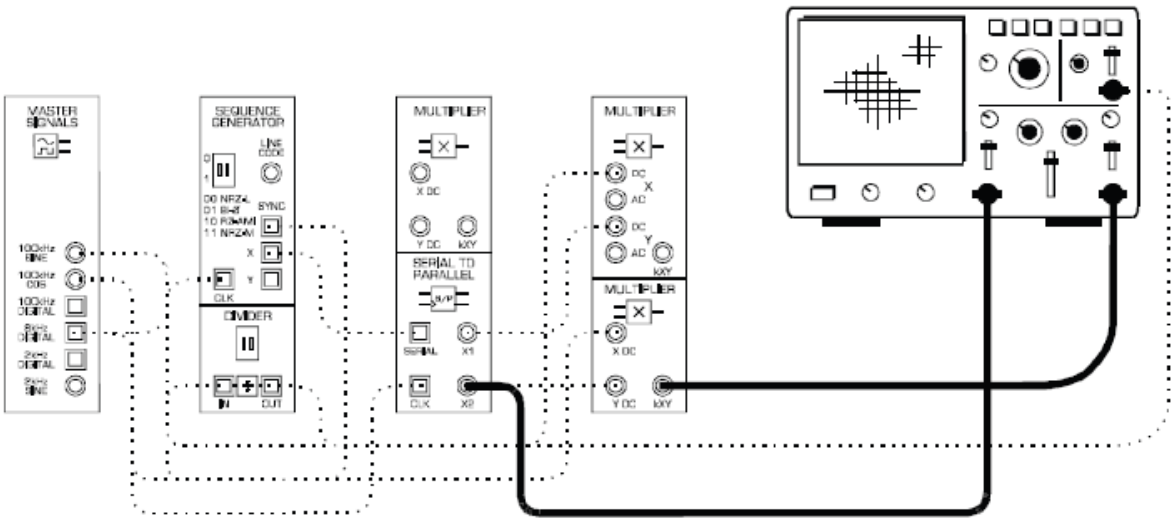

Figure 9: the set-up for the generation of PSK_Q

Figure 9 can be represented by the block diagram in Figure 10 below.

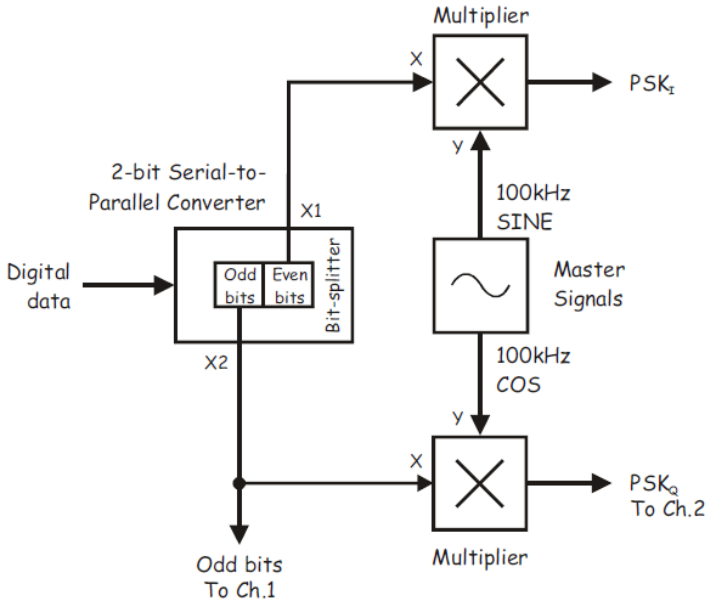

Figure 10: the block diagram of Figure 9

9. Activate the scope's Sweep Multiplier to view the signals more closely.
10. Use the scope's Horizontal Position control to locate a transition in the data sequence.
11. Examine the carrier and look closely at the way it changes at the sequence's transitions.

Question 3

What type of signal is present on the Multiplier's output?

12. Deactivate the scope's Sweep Multiplier and return the scope's Timebase control to the 0.5 ms/div setting.
13. Modify the set-up as shown in Figure 11 below.

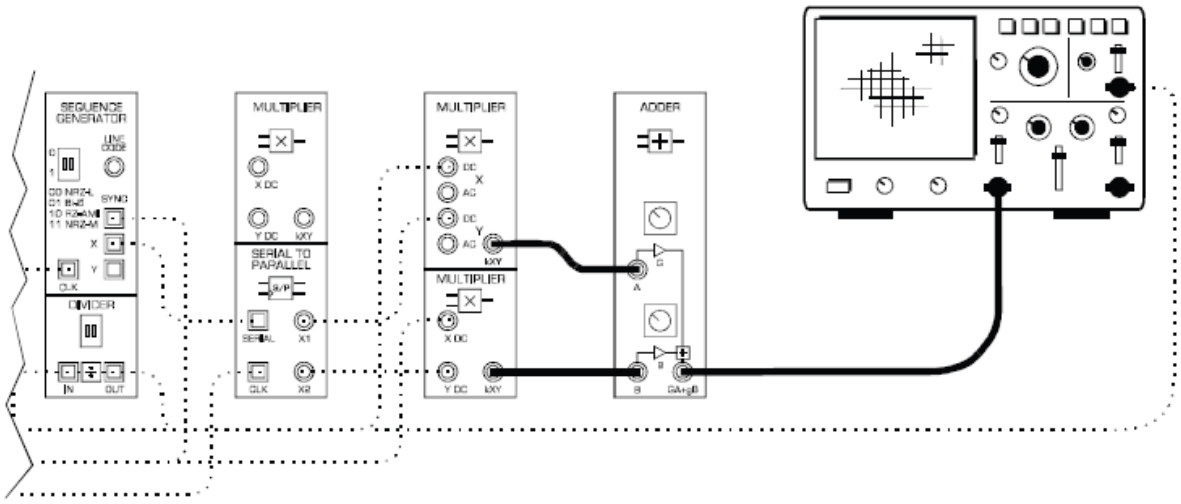

Figure 11: the set-up for a QPSK signal generation

The set-up in Figure 11 can be represented by the block diagram in Figure 12 below. The Adder module is used to add the PSK_I and PSK_Q signals. This turns the set-up into a complete QPSK modulator.

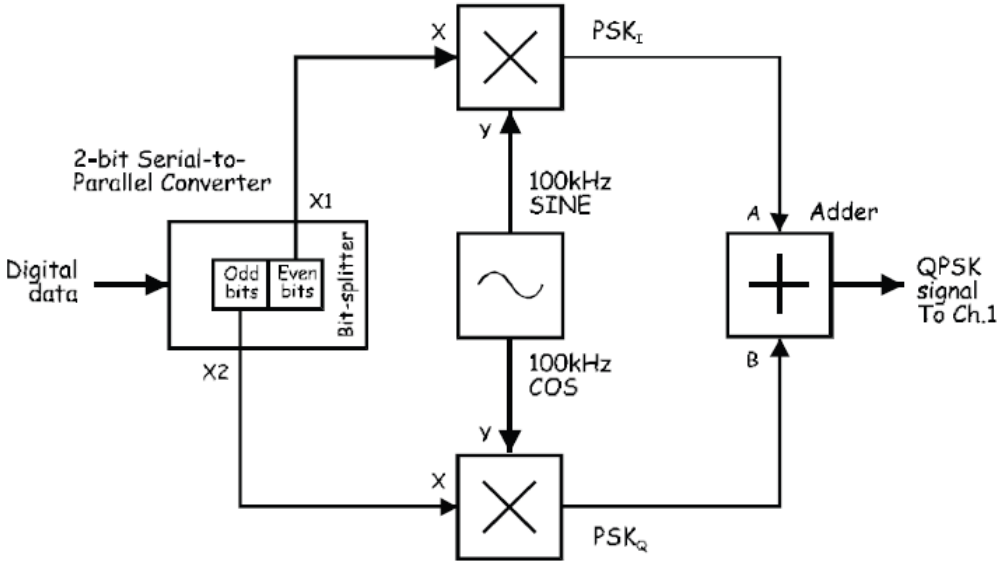

Figure 12: the block diagram of Figure 11

14. Turn the Adder module's G control fully anti-clockwise.
    Note: This removes the $BPSK_I$ signal from the signal on the Adder module's output.
15. Adjust the Adder's g control to obtain a 4 V_{p-p} output.
16. Disconnect the patch lead to the Adder module's B input.
    Note: This removes the $BPSK_Q$ signal from the signal on the Adder module's output.
17. Adjust the Adder's G control to obtain a 4 V_{p-p} output.
18. Reconnect the patch lead to the Adder module's B input.

Question 4
According to the theory, what type of digital signal transmission is now present on the Adder's output?

19. Set the scope's Timebase control to the 0.2 ms/div position.
20. Activate the scope's Sweep Multiplier to view the signal more closely.
21. Use the scope's Horizontal Position control to examine the signal from beginning to end.

Question 5
Why is there only one sinewave when the QPSK signal is made up of two BPSK signals?

Part B – Using phase discrimination to pick-out one of the QPSK signal's BPSK signals
It's not possible to implement both a QPSK modulator and demodulator with one Emona Telecoms-Trainer 101. However, it is possible to demonstrate how phase discrimination is used by a QPSK demodulator to pick-out one or other of the two BPSK signals that make up the QPSK signal. The next part of the experiment lets you do this.

1. Deactivate the scope's Sweep Multiplier and return the scope's Timebase control to the 1 ms/div setting.
2. Locate the Tuneable LPF module and turn its Cut-off Frequency Adjust control fully clockwise.
3. Locate the Phase Shifter module and set its Phase Change control to the 0^o position.
4. Modify the set-up as shown in Figure 13 below.

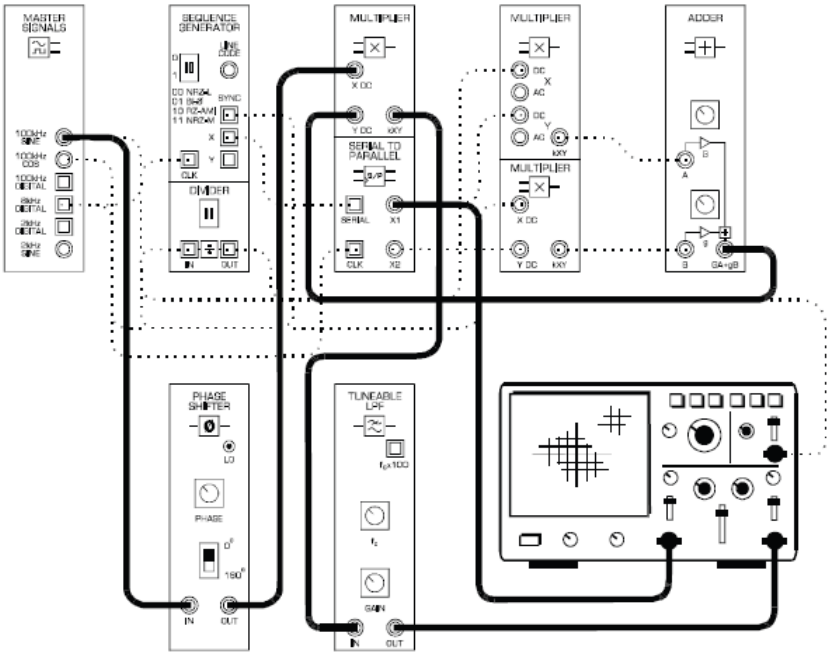

Figure 13: the set-up for a (part of) QPSK demodulation

The additions to this set-up can be represented by the block diagram in Figure 14 below. If you compare the block diagram to Figure 4 in the preliminary discussion, you'll notice that it implements most of one arm of a QPSK demodulator (either I or Q).

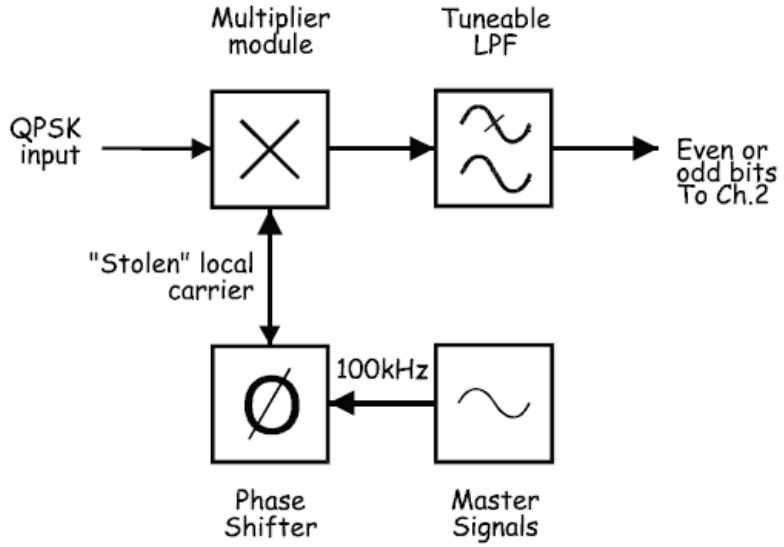

Figure 14: block diagram of Figure 13

5. Compare the even data bits on the Serial-to-Parallel Converter module's X1 output with the data on the output of the Baseband LPF.
6. Vary the Phase Shifter module's Phase Adjust control left and right and observe the effect on the demodulated signal. You are aiming to recover a bipolar (2-level) signal like the original X1 or X2 signals from the Serial-to-Parallel Converter module.
7. Set the Phase Shifter module's Phase Change control to the 180° position and repeat step 6.

Question 6

What is the cause of the 3 and 4 level signals out of the Tuneable LPF during the phase adjustments above? How many different Phase Adjust control positions will give you a bipolar signal?

8. Modify the set-up as shown in Figure 15.

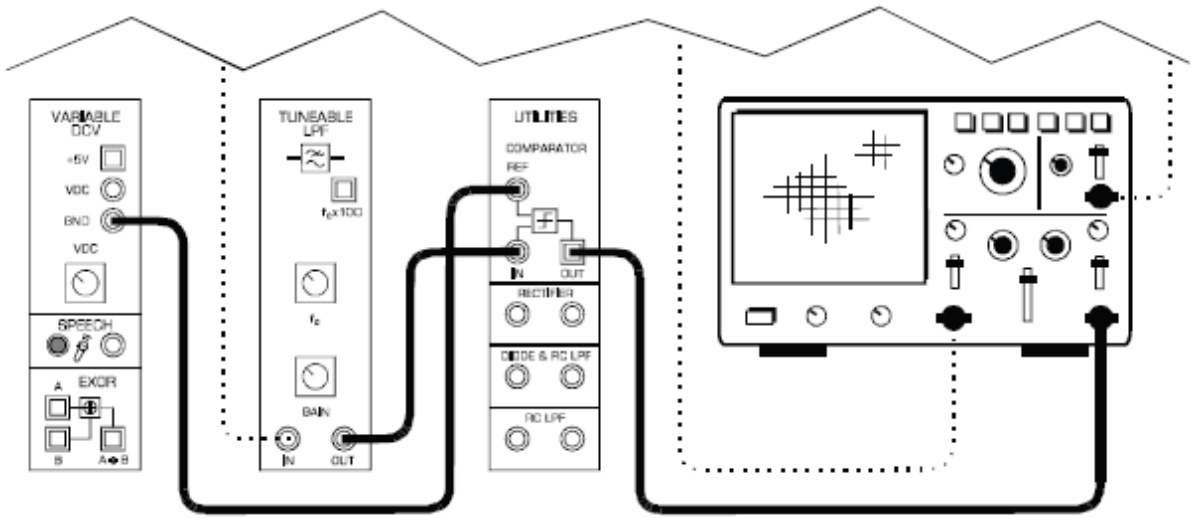

Figure 15: the set-up for a QPSK demodulation (one branch)

The addition of the Comparator on the Utilities module can be represented by the block diagram in Figure 16 below. If you compare this block diagram with Figure 4 in the preliminary discussion, you'll notice that this change completes one arm of a QPSK demodulator.

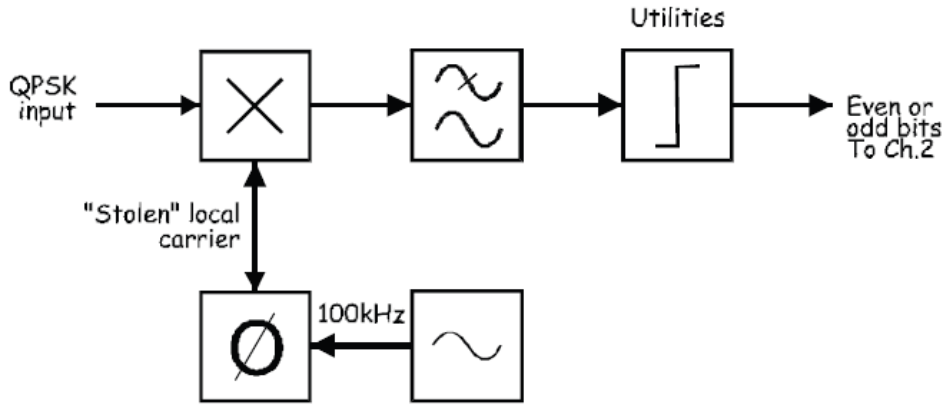

Figure 16: block diagram of Figure 15

9. Set the Phase Shifter module's Phase Change control to the 0° position.
10. Compare the even data bits on the Serial-to-Parallel Converter module's X1 output with the data on the output of the Baseband LPF.
11. Adjust the Phase Shifter module's soft Phase Adjust control until you have recovered the even data bits (ignoring any phase shift).

Question 7

What is the present phase relationship between the local carrier and the carrier signals used to generate the PSK_I and PSK_Q signals?

12. Unplug the scope's Channel 1 input from the Serial-to-Parallel Converter module's X1 output and connect it to its X2 output to view the odd data bits.
13. Compare the odd data bits with the recovered data. They should be different.
14. Set the Phase Shifter module's Phase Change control to the 180° position.
15. Adjust the Phase Shifter module's Phase Adjust control until you have recovered the odd data bits (ignoring any phase shift).

Question 8

What is the new phase relationship between the local carrier and the carrier signals used to generate the PSK_I and PSK_Q signals?

Question 9

Why is your demodulator considered to be only one-half of a full QPSK receiver?